

DERWENT-ACC-NO: 2002-444048

DERWENT-WEEK: 200649

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TITLE: Method and receiver unit for
effecting controlled
synchronization on an
unstable clock pulse system uses
soft synchronization caused
by slightly altering a
generated clock pulse
signal's period to modify this
signal.

INVENTOR: ROTSCH, H; WANNER, D

PATENT-ASSIGNEE: SIEMENS AG[SIEI]

PRIORITY-DATA: 2000DE-1046920 (September 21, 2000)

PATENT-FAMILY:

PUB-NO	PAGES	PUB-DATE
LANGUAGE		MAIN-IPC
US 7082175 B2		July 25, 2006
N/A	000	H04L 007/00
WO 200227990 A2		April 4, 2002
G	022	H04J 003/06
<u>DE 10046920 A1</u>		April 25, 2002
N/A	000	H04L 007/08
US 20020126782 A1		September 12, 2002
N/A	000	H04L 007/00
EP 1325578 A2		July 9, 2003
G	000	H04J 003/06
<u>DE 10046920 C2</u>		August 14, 2003

N/A	000	H04L 007/08
CN 1476691 A		February 18, 2004
N/A	000	H04J 003/06
EP 1325578 B1		April 20, 2005
G	000	H04J 003/06
DE 50105973 G		May 25, 2005
N/A	000	H04J 003/06

DESIGNATED-STATES: CN AT BE CH CY DE DK ES FI FR GB
 GR IE IT LU MC NL PT SE TR
 AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL
 PT SE TR DE FR GB

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-
NO	APPL-DATE	
US 7082175B2	N/A	
2001US-0855899	May 15, 2001	
WO 200227990A2	N/A	
2001WO-DE03471	September 10, 2001	
DE 10046920A1	N/A	
2000DE-1046920	September 21, 2000	
US20020126782A1	N/A	
2001US-0855899	May 15, 2001	
EP 1325578A2	N/A	
2001EP-0978107	September 10, 2001	
EP 1325578A2	N/A	
2001WO-DE03471	September 10, 2001	
EP 1325578A2	Based on	WO
200227990	N/A	
DE 10046920C2	N/A	
2000DE-1046920	September 21, 2000	
CN 1476691A	N/A	
2001CN-0819258	September 10, 2001	
EP 1325578B1	N/A	
2001EP-0978107	September 10, 2001	

EP 1325578B1	N/A	
2001WO-DE03471	September 10, 2001	
EP 1325578B1	Based on	WO
200227990	N/A	
DE 50105973G	N/A	
2001DE-0505973	September 10, 2001	
DE 50105973G	N/A	
2001EP-0978107	September 10, 2001	
DE 50105973G	N/A	
2001WO-DE03471	September 10, 2001	
DE 50105973G	Based on	EP
1325578	N/A	
DE 50105973G	Based on	WO
200227990	N/A	

INT-CL (IPC): G05B019/418, H03L007/07 ,
H04J003/06 , H04L007/00 ,
H04L007/08 , H04L012/413 , H04L025/00 ,
H04L025/40

ABSTRACTED-PUB-NO: US20020126782A

BASIC-ABSTRACT:

NOVELTY - Soft synchronization caused by slightly altering the period of a generated clock pulse signal (a) generated for an application (4) modifies this signal so that a phase difference (c) between this signal and a stable clock pulse signal (b) generated by a phase-locked loop (PLL) (6) on a synchronization signal (S) slowly decreases until both clock pulse signals (a,b) synchronize. The soft synchronization differs only slightly from a

normal operating state.

USE - In field of network automation bus systems like PROFIBUS viz. distributed control systems with multiple slave receiver devices and transmitter devices like head components and bus masters.

ADVANTAGE - Generated clock pulse signals largely retain their period thereby ensuring that applications called up in cycles can be run completely with the required precision. Variations in a first clock pulse generator's period are regulated by the PLL and reproduced on a second clock pulse generator while a phase difference to be compensated for remains constant.

DESCRIPTION OF DRAWING(S) - The drawing shows a phase-locked loop with a secondary controlled clock pulse transmitter.

Generated clock pulse signal a

Application 4

Phase difference c

Stable clock pulse signal b

Phase-locked loop 6

Synchronization signal S

ABSTRACTED-PUB-NO: WO 200227990A

EQUIVALENT-ABSTRACTS:

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CHOSEN-DRAWING: Dwg.3/4

DERWENT-CLASS: T06 U22 U23 W01

EPI-CODES: T06-A06A2; T06-A07A1; U22-D; U22-D01A6;
U23-D01; W01-A04A2;
W01-A04B1; W01-A06B5A; W01-A06E2B;